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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/636,060	08/07/2003	Derick G. Behrends	ROC920030049US1	1005

7590 12/13/2006

Intellectual Property Law Dept.
IBM Corporation, Dept. 917
3605 Highway 52 North
Rochester, MN 55901-7829

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/636,060	BEHRENDS ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *13-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to the present US Application 10/636,060, filed 08/07/2003. Claims 1-21 are presently under examination and pending in the Application.

Specification

The abstract of the disclosure is objected to because it fails to comply with a proper language and format for an abstract of the disclosure. Correction is required. See MPEP § 608.01(b).

The following is a new abstract as suggested by the Examiner:

"A method for testing an integrated circuit (IC), including the steps of selecting a bit from each of a plurality of memory arrays formed on an IC chip, selecting one of the plurality of memory arrays, and storing the selected bit from the selected memory array".

Claim Objections

Claims 13-21 are objected to because of the following informalities:

Claims 13, 15, 17, 19 and 21 in passim recite: "adapted to ...' It has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7-11 and 13-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Liu et al. (US Patent No: 5,781,488), issued: July 14, 1998.

Regarding independent Claims 1, 7, 13, 17, Liu discloses a method and apparatus for testing an integrated circuit (IC), Fig. 2, comprising:

Selecting a bit (memory cell, representing one bit of information) from each of a plurality of memory arrays (41 and 42) formed on the IC chip, Fig. 2. To read out a memory cell, one wordline is selected from among the wordlines in memory arrays 41 and 42. The selected word line activates one row of memory cells. However, only the memory cells connected to the selected bitline pair (shown, for example, as 401C and 403C) will be read.

Selecting one of the plurality of memory arrays (41 or 42), using multiplexer 80 which performs the selection of DB_L /DB_L* and DB_R /DB_R* lines in response to an asserted input signal <A> or <B> from the selected array 41 or 42, respectively. If input signal <A> is asserted, the signals on DB_L /DB_L* lines are passed through for amplification, thus selecting memory array 41. If input signal <B> is asserted, the

signals on DB_R /DB_R* lines are passed through for amplification, thus selecting memory array 42.

Storing the selected bit DO_m from the selected memory array through I/O Sense amplifier 70, which provides the amplified signal on its output terminal DO_m. The output terminal DO_m is in turn fed to an output buffer not shown, Fig. 2. However, the circuit of Fig. 4 shows a sense amplifier stage 10 similar to I/O Sense amplifier 70 coupled to an output buffer stage 20. The output buffer stage 20 comprises a cross coupled pair of 2-input NAND gates, such as a latch for storing the selected bit by receiving SAO1 and SAO2 input signals and providing an output signal on terminal 3.

Regarding Claims 2, 3, 8, 9, selecting a wordline in each of the plurality of memory arrays (41 and 42). To read out a memory cell, one wordline is selected from among the wordlines in memory arrays 41 and 42. The selected word line activates one row of memory cells. However, only the memory cells connected to the selected bitline pair (shown, for example, as 401C and 403C) will be read.

Regarding Claims 4, 5, 10, 11, storing the selected bit from the selected memory array in a latch. The output buffer stage 20 comprises a cross coupled pair of 2-input NAND gates, such as a latch for storing the selected bit by receiving SAO1 and SAO2 input signals and providing an output signal on terminal 3.

Regarding Claims 14-16, 18-21 decoder for generating asserted input signals <A> or <B> coupled to multiplexer 80, for selecting DB_L /DB_L* and DB_R /DB_R* lines for selecting memory arrays 41 and 42, Fig. 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (US Patent No: 5,781,488), issued: July 14, 1998 in view of Jain (US Patent No: 6,853,597), filed: September 26, 2002.

Regarding Claims 6, 12, Liu does not disclose performing the method steps of selecting a bit, selecting one of the memory arrays, and storing the selected bit during an ABIST test. However, in analogous art, Jain discloses an integrated circuit, IC having a plurality of memory banks, including a BIST control unit for testing the plurality of memory banks simultaneously, (see, Jain, Summary of the Invention and Fig. 1).
It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a BIST in the integrated circuit (IC) of Liu, as taught by Jain, for the purpose of testing a plurality of memory banks simultaneously, so as to enhance testing by reducing testing time for an integrated circuit (IC).

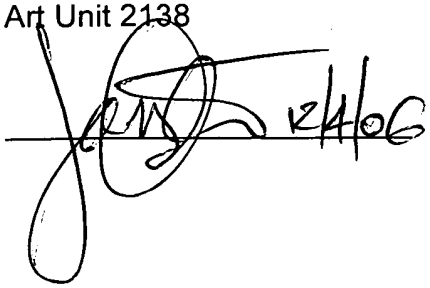
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2138



Date: 4 December 2006
Office Action: Non-Final

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